

CLAIMS

1. A dynamic logic register, comprising:
 - a complementary pair of evaluation devices responsive to a clock signal;
 - a dynamic evaluator, coupled between said complementary pair of evaluation devices at a pre-charged node, that evaluates a logic function based on at least one input data signal;
 - delayed inversion logic that receives said clock signal and that outputs a complete signal being a delayed and inverted version of said clock signal;
 - latching logic, responsive to said clock and complete signals and the state of said pre-charged node, that controls the state of an output node based on the state of said pre-charged node during an evaluation period between an operative edge of said clock signal and the next edge of said complete signal and that otherwise presents a tri-state condition to said output node; and
 - a keeper circuit coupled to said output node.
2. The dynamic logic register of claim 1, wherein said complementary pair of evaluation devices comprises:

a P-channel device having a gate receiving said clock signal and a drain and source coupled between a source voltage and said pre-charged node; and

an N-channel device having a gate receiving said clock signal and a drain and source coupled between said dynamic evaluator and ground.

3. The dynamic logic register of claim 1, wherein said dynamic evaluator comprises a complex logic circuit.
4. The dynamic logic register of claim 1, wherein said delayed inversion logic comprises at least one inverter.
5. The dynamic logic register of claim 1, wherein said delayed inversion logic comprises a series chain of inverters.
6. The dynamic logic register of claim 1, further comprising qualifying logic coupled to said delayed inversion logic and operative to preserve a preceding state of said output node.
7. The dynamic logic register of claim 1, wherein said latching logic comprises:

an N-channel pass device having a gate receiving said complete signal and a drain and source coupled between said pre-charged node and a pull-up control node;

- a first P-channel pull-up device having a gate receiving said complete signal and a drain and source coupled between a source voltage and said pull-up control node;
 - a second P-channel pull-up device having a gate coupled to said pull-up control node and a drain and source coupled between said source voltage and said output node; and
 - a plurality of N-channel pull-down devices coupled between said output node and ground and controlled by said complete signal, said clock signal and said pre-charged node.
8. The dynamic logic register of claim 7, wherein said plurality of N-channel pull-down devices comprises:
- a first N-channel pull-down device having a gate receiving said complete signal, a drain coupled to said output node, and a source;
 - a second N-channel pull-down device having a gate receiving said clock signal, a drain coupled to said source of said first N-channel pull-down device, and a source; and
 - a third N-channel pull-down device having a gate coupled to said pre-charged node, a drain coupled to said source of said second N-channel pull-down device, and a source coupled to ground.

9. The dynamic logic register of claim 7, further comprising additional logic coupled between said source voltage and said second P-channel pull-up device operative to prevent a selected state of said output node.
10. The dynamic logic register of claim 1, further comprising an output buffer/inverter having an input coupled to said output node and an output coupled to an inverted output node.
11. A dynamic latch circuit, comprising:
 - a dynamic circuit that pre-charges a first node while a clock signal is low and that evaluates a logic function for controlling the state of the first node when said clock signal goes high;
 - a delayed inverter receiving said clock signal that provides an inverted delayed clock signal;
 - a latching circuit, coupled to said dynamic circuit and said delayed inverter, that controls the state of an output node based on the state of said first node during an evaluation period beginning when said clock signal goes high and ending when said inverted delayed clock signal next goes low, and that otherwise presents a tri-state condition to said output node; and
 - a keeper circuit coupled to said output node.

12. The dynamic latch circuit of claim 11, wherein said dynamic circuit comprises:
 - a P-channel device coupled to said first node that pre-charges said first node while said clock signal is low;
 - a logic circuit, coupled to said first node, that evaluates said logic function; and
 - an N-channel device, coupled to said logic circuit, that enables said logic circuit to evaluate said logic function when said clock signal goes high.
13. The dynamic latch circuit of claim 11, wherein said delayed inverter comprises a series chain of inverters.
14. The dynamic latch circuit of claim 11, wherein said latching circuit comprises:
 - an N-channel device that couples a second node to said first node when said inverted delayed clock signal is high;
 - a P-channel device that pulls said second node high while said inverted delayed clock signal is low; and

a stack of devices coupled to said output node,
including a pull-up device that pulls said output
node high when said second node is low and a
plurality of pull-down devices that pull said
output node low during said evaluation period if
said first node is high.

15. The dynamic latch circuit of claim 11, further
comprising qualifying logic coupled to said delayed
inverter and additional logic provided within said
latching circuit to prevent a predetermined logic
state of said output node.
16. A method of dynamically registering an output signal,
comprising:

pre-setting a first node while a clock signal is in a
first logic state;

dynamically evaluating a logic function to control the
logic state of the first node when the clock
signal transitions to a second logic state;

delaying and inverting the clock signal and providing
a delayed inverted clock signal;

latching a logic state of an output node based on the
logic state of the first node determined during
an evaluation period beginning when the clock
signal transitions to the second logic state and
ending with the next corresponding transition of
the delayed inverted clock signal; and

maintaining the logic state of the output node between evaluation periods.

17. The method of claim 16, wherein said pre-setting a first node comprises pre-charging the first node to a high logic state.
18. The method of claim 16, further comprising buffering and inverting the output node.
19. The method of claim 16, wherein said maintaining the logic state of the output node comprises presenting a tri-state condition to the output node and coupling a keeper circuit to the output node.
20. The method of claim 16, the first logic state being a low logic state and the second logic state being a high logic state, wherein said latching a logic state of an output node comprises:

passing a logic state of the first node to a pull-up control node while said delayed inverted clock signal is in a high logic state;

pulling the pull-up control node to a high logic state while said delayed inverted clock signal is in a low logic state;

pulling the output node to a high logic state if the pull-up control node is in a low logic state; and

pulling the output node to a low logic state if the
first node is in a high logic state during an
evaluation period.